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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PASIA, REDENTOR M	
ART UNIT	**PAPER NUMBER**
2416	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,395	BURTON ET AL.	
	Examiner	Art Unit	
	REDENTOR M. PASIA	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on 03/23/2009 has been entered. Claims 19-20 and 23 have been amended. No claims have been canceled or added. Claims 19-23 are still pending in this application, with claims 19 and 23 being independent.

Response to Arguments

2. Applicant's arguments with respect to claims 19-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 19 and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Brightman et al. (US 7,100,020; hereinafter Brightman) in view of Rosenthal et al. (US 5,740,406; hereinafter Rosenthal).

As to claim 19, Brightman shows a device (Figure 2, packet switch 201) comprising:

first circuitry (Figure 16, Fabric Processor 303) to generate a packet (Figure 16-18, col. 34, lines 29-46; note Tx fabric processor 1605 (part of Fabric Processor 303), makes a fabric frame 1801 based on headers 1803, 1805 and payload 1807)

based on packet header data received from and generated by a micro-engine (Figure 16-18; col. 35, lines 14-29; note that header 1805 is received from and generated by header generator 1709) and packet payload data from a memory controller (Figure 16-18; col. 35, lines 14-29; note payload 1807 is DMA'ed via path 1620 from buffer memory 229; col. 5, lines 13-22; note that DMA engine handles the DMA processes involving the transmit processor, buffer manager, and local memory.)

wherein the packet payload data bypasses the micro-engine (Figures 16-18; col. 35, lines 14-29; note that the header and the payload originate from different circuits and thus, the payload being DMA'ed from the buffer memory bypasses the header generators), the first circuitry comprising

second circuitry (Figure 17, header and payload merge 1711) to receive the packet payload data from the memory controller (Figure 16-18; col. 35, lines 14-29; note

payload 1807 is DMA'ed via path 1620 from buffer memory 229; col. 5, lines 13-22; note that DMA engine handles the DMA processes involving the transmit processor, buffer manager, and local memory.), and to store the packet payload data in first-in first-out (FIFO) circuitry (Figure 17; col. 35, lines 14-29; note the use of FIFO 1713 for temporarily storing payloads received from path 1620 in order to deal with delays).

Even though, Brightman shows the use of a FIFO buffer in receiving payload in order to deal with delays, as discussed above, Brightman does not specifically show the details of a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Rosenthal. Specifically, Rosenthal shows a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for the packet payload data (Figure 7; col. 16, line 34 to col. 17, line 42; note pointers are utilized to define the positions of the beginning and end of the individual FIFO buffers 39 and the beginning and end of the data; further note that a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent.) such that alignment of the packet payload data matches the start lane in the FIFO circuitry (Figure 7; col. 16, line 34 to col. 17, line 42; note the use of such pointers allows alignment of data with corresponding FIFO positions).

In view of the above, having the system of Brightman, then given the well-established teaching of Rosenthal, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Brightman as taught by Rosenthal, in order to allow an application know that sufficient space will be available for a given operation (col. 17, lines 15-16).

As to claim 23, Brightman shows a method (Figure 2, note process/method performed by packet switch 201) comprising:

receiving packet header data generated by a micro-engine (Figure 16-18, col. 34, lines 29-46; note Tx fabric processor 1605 (part of Fabric Processor 303), makes a fabric frame 1801 based on headers 1803, 1805 and payload 1807; col. 35, lines 14-29; note that header 1805 is received from and generated by header generator 1709);

storing the packet header data in the FIFO queue (Figure 17; note that assembled frame 1801 including generated packet header 1805 is stored in FIFO 1717);

receiving packet payload data from a memory controller (Figure 16-18, col. 34, lines 29-46; note Tx fabric processor 1605 (part of Fabric Processor 303), makes a fabric frame 1801 based on headers 1803, 1805 and payload 1807; note payload 1807 is DMA'ed via path 1620 from buffer memory 229; col. 5, lines 13-22; note that DMA engine handles the DMA processes involving the transmit processor, buffer manager, and local memory.),

wherein the packet payload data bypasses the micro-engine (Figures 16-18; col. 35, lines 14-29; note that the header and the payload originate from different circuits and thus, the payload being DMA'ed from the buffer memory bypasses the header generators); and

storing the packet payload data in a first-in first-out (FIFO) queue (Figure 17; col. 35, lines 14-29; note the use of FIFO 1713 for temporarily storing payloads received from path 1620 in order to deal with delays).

Even though, Brightman shows the use of a FIFO buffer in receiving payload in order to deal with delays, as discussed above, Brightman does not specifically show the details of tracking a start lane in the FIFO queue indicating a start of free space in the FIFO queue, and determining a starting lane for the packet payload data such that alignment of packet payload data matches the start lane in the FIFO queue.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Rosenthal. Specifically, Rosenthal shows a start lane in the FIFO queue indicating a start of free space in the FIFO queue, and determining a starting lane for the packet payload (Figure 7; col. 16, line 34 to col. 17, line 42; note pointers are utilized to define the positions of the beginning and end of the individual FIFO buffers 39 and the beginning and end of the data; further note that a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent.) such that alignment of packet payload data matches the start lane in the FIFO queue (Figure 7; col. 16, line 34 to col. 17, line 42; note the use of such pointers allows alignment of data with corresponding FIFO positions).

In view of the above, having the system of Brightman, then given the well-established teaching of Rosenthal, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Brightman as taught by Rosenthal, in order to allow an

application know that sufficient space will be available for a given operation (col. 17, lines 15-16).

6. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Brightman et al. (US 7,100,020; hereinafter Brightman) in view of Rosenthal et al. (US 5,740,406; hereinafter Rosenthal) in further view of Lincoln et al. (US 6,829,240; hereinafter Lincoln).

As to claim 20, modified Brightman shows all of the elements except logic to synchronize receipt of the packet header data from the micro-engine and the packet payload data from the memory controller, to store the packet header data in the FIFO circuitry, and to transfer the packet header data and packet payload data from the FIFO circuitry to a destination specified in the packet header.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Lincoln. Specifically, Lincoln shows logic (Lincoln: Figure 3-4, 6) to synchronize receipt of the packet header data from the micro-engine and the packet payload data from the memory controller (Lincoln: col. 7, lines 45-63; the ATM header 189 is read from the control memory 38 as indicated at 190. This is the header that was previously provided as at 110 in FIG. 4. This header is transferred as at 192. The FIFO address 193 in the control memory 38 corresponding to the ATM header is then read from the control memory 38 as indicated at 194 in FIG. 6. This indicates where, in host memory space for the host transmit FIFO 150, the payload for the cell (identified by the ATM header read at 190) is located. Note that synchronization was performed in the above manner.)

to store the packet header data in the FIFO circuitry (Lincoln: col. 6, lines 22-25; The header value and the protocol information in the VCC 2 block are read from the control memory 38 as indicated at 108 and 109 respectively in FIG. 4. The header value is then transferred to the transmit FIFO 48 in FIG. 2 as indicated at 110 in FIG. 4), and

to transfer the packet header and packet payload data from the FIFO circuitry (Lincoln: Figure 2; col. 4, lines 42-54; the recombined cell (header and the payload) is passed to the transmit cell interface line 45) to a destination specified in the packet header (Lincoln: col. 4, lines 4-17; The header indicates the path which is being followed to pass the cells to a central office 22 and toward a desired destination.).

In view of the above, having the system of modified Brightman, then given the well-established teaching of Lincoln, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Brightman as taught by Lincoln, in order to minimize the complexity and cost of the system by utilizing the process of streaming data transmitted from, and is received, in FIFO's (col. 2, lines 55-58).

7. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Brightman et al. (US 7,100,020; hereinafter Brightman) in view of Rosenthal et al. (US 5,740,406; hereinafter Rosenthal) in further view of An et al. (US 6,061,361; hereinafter An).

As to claim 21, modified Brightman shows the micro-engine (as discussed above), however, modified Brightman does not specifically show that the micro engine is a direct memory access (DMA) controller send queue to transmit requests and receive responses.

However, the above-mentioned claim limitations are well-established in the art as evidenced by An. Specifically, An shows a direct memory access (DMA) controller send queue (Figure 2; RX DMA Agent 28, 32) to transmit requests and receive responses (Figure 3; col. 3, lines 33 to 67; RX DMA agent sends a request signal and waits for a grant signal (claimed response).).

In view of the above, having the system of modified Brightman, then given the well-established teaching of An, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Brightman as taught by An in order to enable the data controller to selectively grant access for a specific activity that may require access to one or more buses, even if multiple requests are received simultaneously (col. 2, lines 7-10).

8. **Claim 22** is rejected under 35 U.S.C. 103(a) as being unpatentable over Brightman et al. (US 7,100,020; hereinafter Brightman) in view of Rosenthal et al. (US 5,740,406; hereinafter Rosenthal).in further view of Cherukuri (US 5,878,217; hereinafter Cherukuri).

As to claim 22, modified Brightman shows the micro-engine (as discussed above), however, modified Brightman does not specifically show that the micro engine is a direct memory access (DMA) controller receive queue to transmit response and receive requests.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Cherukuri. Specifically, Cherukuri shows a direct memory access (DMA) controller receive queue (Figure 2, DMA Controller 206) to transmit response and receive

requests (Note that arrows indicate that DMA controller 206 receives DMA requests and transmits DMA acknowledgement (claimed response).).

In view of the above, having the system of modified Brightman, then given the well-established teaching of Cherukuri, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Brightman as taught by Cherukuri in order to keep the data in the proper sequence since switching may cause the order of the data to be processed out of its intended sequence (col. 2, lines 36-38).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to REDENTOR M. PASIA whose telephone number is (571)272-9745. The examiner can normally be reached on M-F 7:00am to 3:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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